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UTILITY PATENT APPLICATION TRANSMITTAL
(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. : 34556/JFO/B600
Inventor(s) : Yi-Hsien HAO, Scott McDANIEL, John K. LENELL, and Andrew M. NAYLOR
Title : MEMORY STRUCTURE
Express Mail Label No. : EL497770331US

ADDRESS TO: Assistant Commissioner for Patents
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Washington, D.C. 20231

Date: January 27, 2000

1. X **FEE TRANSMITTAL FORM** *(Submit an original, and a duplicate for fee processing).*

2. **IF A CONTINUING APPLICATION**

   ___ This application is a of patent application No. .

   X This application claims priority pursuant to 35 U.S.C. §119(e) and 37 CFR §1.78(a)(4), to provisional Application Nos. 60/117,481 (CPH Docket No. 33571) and 60/127,147 (CPH Docket No. 34379).

3. **APPLICATION COMPRISED OF**

   Specification
   24 Specification, claims and Abstract (total pages)

   Drawings
   7 Sheets of drawing(s) (FIGS. 1 to 9)

   Declaration and Power of Attorney
   ___ Newly executed
   X No executed declaration
   ___ Copy from a prior application (37 CFR 1.63(d))(for continuation and divisional)

4. ___ **Microfiche Computer Program** *(Appendix)*

5. ___ **Nucleotide and/or Amino Acid Sequence Submission** *(if applicable, all necessary)*
   ___ Computer Readable Copy
   ___ Paper Copy (identical to computer copy)
   ___ Statement verifying identity of above copies

6. **ALSO ENCLOSED ARE**
   ___ Preliminary Amendment
   ___ A Petition for Extension of Time for the parent application and the required fee are enclosed as separate papers
   ___ Small Entity Statement(s)
   ___ Statement filed in parent application, status still proper and desired
   ___ Copy of Statement filed in provisional application, status still proper and desired

UTILITY PATENT APPLICATION TRANSMITTAL
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Docket No.: 34556/JFO/B600

____ An Assignment of the invention with the Recordation Cover Sheet and the recordation fee are enclosed as separate papers

____ This application is owned by pursuant to an Assignment recorded at Reel , Frame

____ Information Disclosure Statement (IDS)/PTO-1449

____ Copies of IDS Citations

____ Certified copy of Priority Document(s) *(if foreign priority is claimed)*

____ English Translation Document *(if applicable)*

_X_ Return Receipt Postcard (MPEP 503) (should be specifically itemized).

____ Other

7. **CORRESPONDENCE ADDRESS**

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JFO/llb

09425651 "042700

MEMORY STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATIONS

This patent application claims the benefit of the filing date of United States Provisional Patent Application Serial No. 60/117,481, filed January 27, 1999, entitled ETHERNET SWITCHING and United States Provisional Patent Application Serial No. 60/127,147, filed March 31, 1999, entitled ETHERNET SWITCHING, the entire contents of both of which are expressly incorporated herein by reference.

BACKGROUND OF THE INVENTION

The invention herein relates to packet-based network switches; particularly to high-speed multiport packet-based network switches; and more particularly to memory structures, and associated operational techniques, for high-speed multiport packet based network switches.

Present-day throughput demands on packet-based switched networks have created the necessity for switches exhibiting increasingly higher performance. It is most desirable to achieve the transmission speed of the physical transport medium, i.e. to be close to "wire speed." For high-speed LAN protocols, including those collectively called "Fast Ethernet," switches typically associated with operations incorporating OSI Reference Model Layer 2 (Data Link Layer) and Layer 1(Physical Layer) are employed to meet the performance requirements reliably and economically. As the complexity of such devices increases, however, significant trade-offs, for example, between performance, scalability, and affordability may arise.

SUMMARY OF THE INVENTION

The present invention includes a shared memory structure which has an Address Resolution Table for resolving addresses in a packet-based network switch; and a Packet Storage Table that is adapted to receive a packet for storage in the packet-based network switch.

In another aspect of the invention, the Address Resolution Table is implemented using an associative memory structure, including, without limitation, a direct-mapped (one-way associative) memory. This memory may be searched for destination addresses using a destination address key direct-mapped address search. The shared memory structure also can include a Transmit Descriptor Table. It is desirable to have a Transmit Descriptor Table corresponding with a packet-based network transmit port.

Furthermore, the shared memory structure may include a Free Buffer Pool having multiple memory buffers, each having a pre-determined number of memory locations associated therewith. A bit-per-buffer technique can be used for tracking buffer status also can be used.

The invention can be practiced in a packet-based network switch which implements IEEE Standard 802.3 communication protocols. In the switch, the associated Address Resolution Table and the Packet Storage Table also employ a shared memory structure. The switch may have multiple ports and, indeed, it is contemplated that a switch, according to the present invention, have four, eight, nine, or more, such ports.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is an illustration of a multi-port packet-based switch having an embodiment of the present invention;

FIG. 2 is an illustration of one memory block configuration having an embodiment of the shared memory structure according to the invention herein;

FIG. 3 is an illustration of plural memory blocks, each having the memory structure illustrated in FIG. 2;

FIG. 4 is an illustration of one embodiment of an ARL Address Table of the present invention;

FIG. 5 is a table illustrative of storage for an individual 66-byte packet in the context of the invention herein;

FIG. 6 is a an illustration of a packet data bit mapping table implementing an embodiment of the present invention;

FIG. 7 is an illustration of a transmit descriptor pointer address as implemented by an embodiment of the present invention;

FIG. 8 is a block diagram of an embodiment of the free buffer manager;

FIG. 9 is a state diagram illustrating the operation of one embodiment of the buffer control finite state machine in FIG. 8.

DETAILED DESCRIPTION OF THE INVENTION

The present invention is described in the context of the communication protocol defined by IEEE Standard 802.3, and supplemented, for example, by IEEE Standard 802.3u, which also is known as 100Base-T or "Fast Ethernet." Thus, embodiments of the present invention can be implemented in hybrid, or dual speed, 10/100BASE-T devices. One skilled in the art would realize that this contextual description is exemplary, and that the invention can be practiced in the context of other packet-based communication protocols, and at wire speeds surpassing those embodied, for example, by the 100BASE-T standard. Also, a skilled artisan would be familiar with the IEEE Standard 802.3, and thus would require no additional elaboration herein of these Standards to practice the invention. Furthermore, such IEEE Standards 802.3 are incorporated by reference herein in their entirety.

A packet-based Layer 2 switch typically includes fundamental components such as physical layer transceivers (PHY), media access controllers (MAC), an address management unit, a packet

switching fabric, random access memory, and the like. The physical transceiver layer, MAC, and other aspects of a packet-based switch can be defined by standards such as, for example, the IEEE 802.3 group of specifications (hereinafter referred to as "Ethernet" or, where appropriate, "Fast Ethernet"). The integration of some of these components is known in the art. However, total integration of all components onto a single chip may create performance trade-offs, depending, for example, upon the complexity of the switch. As the number of supported nodes increases, it becomes more difficult to meet power requirements and die size constraints, and still operate at, or near, wire speeds.

Among the functions supported, a Layer 2 switch resolves the destination of frames received at an ingress port by building a table of destination addresses and an associated egress port. An Ethernet destination address typically is a 48-bit value. Therefore, building a direct mapping for each possible address can require 2^{48} memory locations. Recognizing that only a small number of the 2^{48} addresses may be used in a LAN system, it is desirable to reduce the memory required to store the addresses, and to minimize the probability of an address search miss. Techniques to realize these goals include the use of a content-addressable memory (CAM), binary search algorithms, and hash tables with chain entries of depth greater than 1. However, such techniques can be costly to implement, and can degrade the frame rate resolution of destination addresses such that operation at wire speed can be difficult to maintain under some circumstances.

FIG. 1 illustrates a packet-based multiport switch 1 which includes an integrated switching controller 2, and a memory 3, external to switching controller 2. According to an embodiment of the present invention, it is contemplated that Packet Data Storage Table 4 be co-located with Address Resolution Table 5. In particular, it is most desirable that Packet Data Storage

Table 4 share memory with ARL Table 5. Further, memory 3 also can include Transmit Descriptor Table 6. Integrated switching controller 2 can include switching fabric 7, free buffer pool memory 8, free buffer pool memory manager 9, and MAC/PHY components 10a, 10b, and 10c.

An advantage of having a shared memory structure 3 as contemplated by the present invention is the reduction in device pin count and in system implementation costs. An advantage of implementing the invention as a direct-mapped address table is that the number of memory accesses required for address resolution per Ethernet frame can be about one cycle per Ethernet frame for address learning, and about one cycle per Ethernet frame for address resolution. Furthermore, the memory addressing logic required to access the ARL table can be minimized. It is desirable to use a direct-mapped/one-way associative address table, indexed by a key, for example, extracted from the thirteen least significant bits of the 48-bit Ethernet frame destination address field.

In one embodiment of the invention, ARL Table 5 may be used without a shared memory structure. In this case, it is desirable for the table to be configured as an one-way associative, i.e., direct mapped, memory. In embodiments of the invention in which the ARL Table 5 is shared with Table 4, Table, 6, or both, as well as with pool memory 8, it may be desirable to use another type of memory structure, including, without limitation, an ***n***-way associative memory, a hash table, binary searching structure, and a sequential searching structure. One skilled in the art could readily select the appropriate a search technique for a given structure.

By using the one-way associative memory configuration for ARL Table 5, address resolution can be made simple, and memory access expeditious, thereby reducing the switching bandwidth needed to determine the packet destination port address, and to

allow the Packet Data Storage Table 4 to be co-located with ARL Table 5. This direct-mapped configuration of ARL Table 5 reduces the switching bandwidth needed to determine the packet destination port address, and permits an associated device to operate at, or near, wire speed.. Also, the direct mapping can be a significant factor in implementing the single, shared memory structure for the ARL Table 5 and Packet Data Storage Table 4, which facilitates switch operation at wire speeds.

The implementation of shared memory 3 and the implementation of a direct-mapped ARL Table 5, alone and together, are more desirable techniques to increase bandwidth than merely increasing clock frequency because operations using faster clock frequencies typically result in increased power requirements, and a need for faster memory which, itself, can add to the cost, and complexity, of the associated product. Thus, where it is desired to contain device power requirements and to minimize switch cost, the aforementioned approaches are beneficial.

By using a preselected portion of the packet destination address as an index into ARL Table 5, a address match can be resolved quickly, and the packet passed to the appropriate port for transmission. This destination address key direct-mapped address search enables multiport packet-based switch 1 to be operable, for example, at wire speed in full-duplex, non-blocked, 100Base-TX operations. One skilled in the art would realize that the contemplated invention can be practiced in environments other than 100BASE-T environments and at wire speeds in excess of 100 Mb/s.

FIG. 2 provides an illustration of one embodiment of a memory map 100 that can implement a block of memory such as memory 3 in FIG. 1. At first address locations 11 (00-CF), there exists a single buffer 12 for an individual packet. A transmit descriptor table, similar to Transmit Descriptor Table 6 in FIG. 1, is created by allocating sufficient memory beginning at first

memory location 13 (D0) to second memory location 15 (D8) which encompass port 0 transmit descriptor 14 through port 8 transmit descriptor 16. Also, an address resolution table similar to ARL Table 5 in FIG. 1, can be created by allocating a memory segment 17 such that it contains a preselected number of ARL table entries 18 (e.g., 32 entries).

With one buffer per packet, only one transmit descriptor read per packet is performed, eliminating multiple memory accesses to find, for example, a linked list of buffers in an external memory. Given the starting address of the frame and the length of the frame in the transmit descriptor, only one access is executed in order to locate the entire packet to be transmitted. In a typical linked-list buffer approach, employing a small, fixed buffer block size, additional transmit descriptor reads may be required in order to locate each subsequent block. Each additional read signifies an undesirable reduction in available bandwidth.

Furthermore, the single buffer per packet approach as contemplated herein reduces the number of buffers that need to be searched. A skilled artisan would appreciate the significant bandwidth savings that can be attributed to the one buffer per packet approach. The single buffer-per-packet technique enhances the feasibility of the bit-per-buffer free buffer pool tracking technique, as well, and the need to search a large buffer pool structure can be mitigated or eliminated. In view of the foregoing, it can be seen how embodiments of the contemplated invention effect switch operation at, or near, wire speed.

FIG. 3 is illustrative of the scalability of this shared memory structure in that the memory structure described in FIG. 2 can be allocated in address range 19 of memory block 20. A skilled artisan would realize that one or more such blocks can be used to achieve the desired design criteria.

FIG. 4 illustrates one embodiment of the direct-mapped address table indexing using, for example, a 13-bit key derived from the 48-bit MAC address value, i.e., the Ethernet frame destination address field 21. As previously described, the least significant bit 23 of address value 21 is mapped to the least significant bit 24 of key 22. In this example, the address table entries, therefore, are offset in the address space from the index by $F0_h$. The most significant bit location 25 can obtain its value 26 from bit 35 of the corresponding MAC address value 21. If desired, a fourteenth bit from MAC address 21 can be used to provide a bit value 28 for the most significant bit 27 for key 22.

Thus, a packet-based switch implementing the shared memory structure according to the contemplated invention performs one memory read for address resolution, and one memory write for address learning, to the address table for each frame received. The reduced overhead provided by embodiments of present invention leads to a reduction in memory accesses per Ethernet frame (in this example, a frame is 64 bytes in length, and the associated bus width is 64 bits). The number of such memory accesses can be characterized as: one cycle per frame for address resolution; one cycle per frame for address learning; one cycle per frame for transmission read; one cycle per frame for transmission write; one cycle per eight bytes for a frame data read; and one cycle per eight bytes for a frame data write.

The single access for both read and write can be attributed to the single-entry direct-mapped address table. Using this configuration, each MAC address maps to a single location in the address table. Therefore, only one access may be needed to read or write the MAC address. A single-entry direct-mapped address table may increase the probability of address collisions. However, the probability of these collisions can be reduced by mapping over a larger number of MAC address bits, such as the 14

bits illustrated in FIG. 4. The single MAC address read and write for each Ethernet frame can contribute to the ability of switch 1, in FIG. 1, to operate at wire speed, in a full-duplex, non-blocking manner.

To further enhance the functionality of switch 1 in FIG. 1, a transmit descriptor request may be made during the transmission of a previous frame, thereby removing the transmit descriptor reads from the generation of latency. Also, it is desirable that a FIFO structure be used so that a first portion of the FIFO data can be read to initiate transmission while the remaining portion of the FIFO structure is still receiving data.

In one embodiment of the invention, memory structure 3 of Figure 1 employs a 64-bit memory bus operating with a 66 MHz system clock. Throughput can further be enhanced by implementing a memory arbitration scheme such as a weighted priority round-robin memory arbitration technique. This technique enhances the memory structure's quantization and prioritization of memory accesses, further reducing latency loss and bandwidth requirements.

An embodiment of the present invention contemplates the implementation of a memory arbiter that, in this example, provides arbitration for six types of memory accesses. The arbiter sets priority between the Ethernet ports as highest priority and that of an expansion port as the lowest priority for each of the memory access types. Each access type is also prioritized such that the access type meets the latency requirement for maintaining wire speed switching of the supported function. The selected arbitration and associated priority are as shown in Table 1.

TABLE 1

Access Type	Priority	Cycles/Access	Access/Frame #
Frame Data Writes	1	4	2
Frame Data Reads	2	4+2 Turnaround	2
Transmit Descriptor Read	3	1+2 Turnaround	1
Destination Address Read	4	1+2 Turnaround	1
Transmit Descriptor Write	5	1	1
Source Address Write	6	1	1
*64-byte Ethernet Frame			

The cycles/access number refers to the number of system clock cycles required to perform memory access when interfacing, for example, to an external synchronous static RAM in flowthrough mode, with 64-bit data word width.

Data packets can be stored in Packet Data Storage Table 4 of FIG. 1, with a packet data address portion, and a packet data value portion. References to packets are often passed within switch 1, which can, for example, use the upper nine buffer bits of Table 4 as a pointer value. These pointer values are passed between the Free Buffer Manager 9 and ports 10a, 10b, 10c. The data address pointer value can also be passed between the switch Rx ports and the switch Tx ports via the transmit descriptor, which is similar to descriptor 14.

FIG. 5 illustrates how packet data values can be stored. In the example of FIG. 5, a 66-byte packet is stored. As seen in FIG. 5, it is desired to store packet data in 64-bit wide memory segments, such that the efficiencies brought about by the 64-bit wide memory data path are further realized.

FIG. 6 is exemplary of mapping a transmission format to other selected memory formats. Although the format normally used to display Ethernet data is a byte-stream format 40, FIG. 6 also

displays the Ethernet data in a bit-stream format 41, a nibble-stream format 42, a byte-stream format 43 and a word-stream format 44.

In FIG. 1, it is desired that there be one Transmit Descriptor Table 6 for each transmit port. Thus, a switch having multiple ports (e.g., 4, 8, or 9 ports) could use a corresponding number of Transmit Descriptor Tables 6 (e.g., 4, 8, or 9 tables). It is also desired that each Transmit Descriptor Table 6 consist of a circular queue structure, i.e., a FIFO, that can hold a pointer value for each buffer in switch 1. Typically, a circular queue structure (FIFO) has a tail pointer and a head pointer that are maintained in each Tx block. When the values are the same, the queue is empty.

FIG. 7 illustrates the desired structure of a head pointer, a tail pointer, or both. In FIG. 7, head pointer 45 is described in this example, although a tail pointer can have the same structural format. Port ID 46 is desired to be static for each transmit port. Nine-bit pointer value 47, in this particular example, is indicative of the head pointer value. Where a reduced amount of memory is used to implement Table 6 of switch 1 in FIG. 1, then the sixteenth bit, 48, of FIG. 7 can be forced low on all memory accesses, having the effect of wrapping the transmit descriptor queues to fit within the available memory without affecting switch 1 operation.

FIG. 8 is an embodiment of a free buffer manager 50 similar to free buffer manager 9 shown in FIG. 1. Manager 50 can include a buffer free bus controller 51, a pipeline buffer search engine 52, a buffer control finite state machine 53, a buffer bus register 54 and a buffer grant bus controller 55. It is desirable that register 54 be a LIFO and, for the purposes of the description herein, register 54 is an eight-location LIFO. It is the responsibility of manager 50 to "grant" new buffers to ports before a data packet is received, and to collect, or

"free," used buffers from ports that have transmitted a packet. Typically, one grant operation will be needed for each packet received by the switch, and one free operation will be needed for each packet transmitted by the switch.

In an embodiment of the present invention, a fixed number of buffers are employed. Used buffers are those that have been granted to a receive port, but have not yet been returned, or freed, by a transmit port. All of the remaining buffers are designated "unused". It also is the buffer manager's responsibility also to track unused buffers so that they can be granted. Although one simple method to track unused buffers is to maintain a buffer list, such a list may create undesirable space limitations on a switch device because the list area must be long enough to store all of the buffers in a system and, further, each location in the list must be able to store the number of, or a pointer to, any buffer in the system. In a device having 512 list locations, for example, with each location having a corresponding nine-bit pointer, 4608 bits of storage would be required.

By contrast, another embodiment of the invention herein, implementing a bit-per-buffer method of tracking free buffers, reduces the storage requirement to only 512 bits, with each bit corresponding to a specific buffer. Here, a used buffer is indicated by setting the corresponding buffer bit. For example, setting the 368 bit in free buffer pool memory 8 in FIG. 1, can indicate that buffer 368 is currently being used.

Although this method does present an economy of storage and circuit area, it is further desired to employ a pipelined engine 52 to search for buffers in the bit array, such that the impact of "free" operations on search speeds is limited and that fast grant rates are allowed. Register 54 is preferred to be an eight-location LIFO to further increase the peak grant rate of search engine 52. Buffer free bus controller 51 captures

requests 58 for the freeing of buffers, and presents request 59 to search engine 52. In addition, controller 51 can provide a similar request 56 to finite state machine 53. Register 54 also provides a status signal 57 to finite state machine 53 and, in conjunction with request data signal 56 from free bus controller 51, buffer control finite state machine 53 can select one of a set of defined states.

The state diagram of FIG. 9 illustrates the three states of state machine 53 in FIG. 8. These three states can include:

1) SEARCH (61) - search for zero-valued bits that are in the buffer control array, indicating the location of a free buffer;

2) FREE (62) - write a zero to a bit location specified by free controller 51, thus freeing the associated buffer for allocation; and

3) ALLOCATE (63) - write a one value to a bit location that was identified during search state 61 by search engine 52.

Returning to FIG. 8. Buffer Search Engine 52 is preferred to be pipelined in both address and data paths, around the buffer control bit memory array, in order to expedite the identification of available buffers. The eight-location LIFO 54 can store the locations of allocated buffers until they are needed by the Buffer Grant Bus Controller 55. Finally, Buffer Grant Bus Controller 55 waits for requests 59 from the received port for buffers and presents the buffer location 60 if available from the LIFO.

The foregoing merely illustrates the principles of the invention, and it will thus be appreciated that those skilled in the art will be able to devise various alternative arrangements which, although not explicitly described herein, embody the principles of the invention within the spirit and scope of the following claims.

34556/JFO/B600

CLAIMS

What is claimed is:

1. A memory structure, comprising:

a. an Address Resolution Table for resolving addresses in a packet-based network switch; and

b. a Packet Storage Table, the Packet Storage Table adapted to receive a packet for storage in the packet-based network switch, and sharing a preselected portion of memory with the Address Resolution Table.

2. The memory structure of claim 1, further comprising at least one of:

a. a Transmit Descriptor Table being associated with a corresponding packet-based network transmit port; and

b. a Free Buffer Pool having plural memory buffers, each of the plural memory buffers having a pre-determined number of memory locations associated therewith.

3. The memory structure of claim 1 wherein the packet-based network switch implements an IEEE Standard 802.3 communication protocol.

4. The memory structure of claim 3 wherein the switch comprises plural ports.

5. The memory structure of claim 4 wherein the switch comprises at least 8 ports.

6. The memory structure of claim 1 wherein the associative memory structure comprises one of an ***n***-way associative memory, a hash table, a binary search structure, and a sequential search structure.

7. The memory structure of claim 3 wherein the number of memory accesses required per Ethernet frame is one of:

a. one cycle per frame for address resolution;
b. one cycle per frame for address learning;
c. one cycle per frame for transmission read;
d. one cycle per frame for transmission write;
e. one cycle per eight bytes for a frame data read; and
f. one cycle per eight bytes for a frame data write.

8. A memory structure comprising an Address Resolution Table having an associative memory structure, the Address Resolution Table for resolving addresses in a packet-based network switch.

9. The memory structure of claim 8 further comprising a Packet Storage Table, the Packet Storage Table adapted to receive at least one of each of a Packet Data Address and a Packet Data Value.

10. The memory structure of claim 9 further comprising a Transmit Descriptor Table, the Transmit Descriptor Table being associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table adapted to receive a Table Descriptor Address and a Table Descriptor Value.

11. The memory structure of claim 8 wherein the associative memory structure comprises one of a direct-mapped/one-way associative memory structure and a two-way associative memory structure.

12. The memory structure of claim 11 wherein the number of memory accesses required per Ethernet frame is one of:

a. one cycle per frame for address resolution;

b. one cycle per frame for address learning;

c. one cycle per frame for transmission read;

d. one cycle per frame for transmission write;

e. one cycle per eight bytes for a frame data read; and

f. one cycle per eight bytes for a frame data write.

13. A memory structure having a memory block, the memory block comprising at least two of:

a. an Address Resolution Table having an associative memory structure, the Address Resolution Table for resolving addresses in a packet-based network switch;

b. a Transmit Descriptor Table, the Transmit Descriptor Table being associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table adapted to receive a Table Descriptor Address and a Table Descriptor Value; and

c. a Packet Storage Table, the Packet Storage Table adapted to receive at least one of each of a Packet Data Address and a Packet Data Value.

14. The memory structure of claim 13 wherein the associative memory structure comprises one of an ***n***-way associative memory, a hash table, a binary search structure, and a sequential search structure.

15. The memory structure of claim 13 wherein the memory block comprises a shared memory block.

16. The memory structure of claim 13 wherein the Transmit Descriptor Table comprises a FIFO memory structure.

17. The memory structure of claim 16 wherein the FIFO memory structure comprises a circular FIFO memory structure, the FIFO memory structure having a head memory pointer and a tail memory pointer.

18. The memory structure of claim 13 further comprising a Free Buffer Pool having plural memory buffers, each of the plural memory buffers having a pre-determined number of memory locations associated therewith.

19. The memory structure of claim 18, wherein the Free Buffer Pool further comprises a buffer control memory.

20. The memory structure of claim 19, wherein the free buffer pool control memory comprises plural memory bits, ones of the plural data bits uniquely corresponding to ones of the pre-determined number of buffer pool memory locations.

21. The memory structure of claim 18, wherein at least two of the Address Resolution Table, the Transmit Descriptor Table, the Packet Storage Table, and the Free Buffer Pool share a memory block.

22. The memory structure of claim 21 wherein the number of memory accesses required per Ethernet frame is one of:

a. one cycle per frame for address resolution;

b. one cycle per frame for address learning;

c. one cycle per frame for transmission read;

d. one cycle per frame for transmission write;

e. one cycle per eight bytes for a frame data read; and

f. one cycle per eight bytes for a frame data write.

23. The memory structure of claim 18, further comprising a free buffer manager, including:

a. a buffer bus controller;

b. a buffer bus register;

c. a buffer control finite state machine, operably coupled with the bus controller and the bus register; and

d. a buffer search engine, operably coupled with the bus controller, bus register, and finite state machine.

24. The memory structure of claim 23 wherein the buffer bus controller comprises:

a. a buffer free bus controller for detecting a buffer request and present the request to at least one of the finite state machine and the buffer search engine; and

b. a buffer grant bus controller for granting an available free buffer, as indicated by the buffer bus register.

25. The memory structure of claim 23 wherein the buffer search engine comprises a pipelined buffer search engine.

26. The memory structure of claim 23 wherein the buffer bus register comprises a LIFO.

27. The memory structure of claim 26 wherein the LIFO comprises an eight-location LIFO.

28. A packet-based switch comprising a shared memory structure having a Address Resolution Table and a Packet Storage Table.

29. The packet-based switch of claim 28 wherein the switch implements an IEEE Standard 802.3 communication protocol.

30. The packet-based switch of claim 29 wherein the switch comprises plural ports.

31. The packet-based switch of claim 28 wherein the number of memory accesses required per Ethernet frame is one of:

a. one cycle per frame for address resolution;

b. one cycle per frame for address learning;

c. one cycle per frame for transmission read;

d. one cycle per frame for transmission write;

e. one cycle per eight bytes for a frame data read; and

f. one cycle per eight bytes for a frame data write.

32. A packet-based switch having a memory structure, the memory structure comprising at least two of:

a. an Address Resolution Table having an associative memory structure, the Address Resolution Table for resolving addresses in a packet-based network switch;

b. a Transmit Descriptor Table, the Transmit Descriptor Table being associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table adapted to receive a Table Descriptor Address and a Table Descriptor Value; and

c. a Packet Storage Table, the Packet Storage Table adapted to receive at least one of each of a Packet Data Address and a Packet Data Value.

33. The packet-based switch of claim 32, wherein the associative memory structure comprises one of an ***n***-way associative memory, a hash table, a binary search structure, and a sequential search structure.

34. The packet-based switch of claim 32 wherein the memory block comprises a shared memory block.

35. The packet-based switch of claim 32 wherein the Transmit Descriptor Table comprises a FIFO memory structure.

36. The packet-based switch of claim 35 wherein the FIFO memory structure comprises a circular FIFO memory structure, the FIFO memory structure having a head memory pointer and a tail memory pointer.

37. The packet-based switch of claim 32 further comprising a Free Buffer Pool having plural memory buffers, each of the plural memory buffers having a pre-determined number of memory locations associated therewith.

38. The packet-based switch of claim 37, wherein the Free Buffer Pool further comprises a buffer control memory.

39. The packet-based switch of claim 38, wherein the free buffer pool control memory comprises plural memory bits, ones of the plural data bits uniquely corresponding to ones of the pre-determined number of buffer pool memory locations.

40. The packet-based switch of claim 37, wherein at least two of the Address Resolution Table, the Transmit Descriptor Table, the Packet Storage Table, and the Free Buffer Pool share a memory block.

41. The packet-based switch of claim 34 wherein the number of memory accesses required per Ethernet frame is one of:

a. one cycle per frame for address resolution;

b. one cycle per frame for address learning;

c. one cycle per frame for transmission read;

d. one cycle per frame for transmission write;

e. one cycle per eight bytes for a frame data read; and

f. one cycle per eight bytes for a frame data write.

42. The packet-based switch of claim 38, further comprising a free buffer manager, including:

a. a buffer bus controller;

b. a buffer bus register;

c. a buffer control finite state machine, operably coupled with the bus controller and the bus register; and

d. a buffer search engine, operably coupled with the bus controller, bus register, and finite state machine.

43. The packet-based switch of claim 42 wherein the buffer bus controller comprises:

a. a buffer free bus controller for detecting a buffer request and present the request to at least one of the finite state machine and the buffer search engine; and

b. a buffer grant bus controller for granting an available free buffer, as indicated by the buffer bus register.

44. The packet-based switch of claim 42 wherein the buffer search engine comprises a pipelined buffer search engine.

45. The packet-based switch of claim 42 wherein the buffer bus register comprises a LIFO.

46. The packet-based switch of claim 45 wherein the LIFO comprises an eight-location LIFO.

47. The packet-based switch of claim 33 wherein the switch implements an IEEE Standard 802.3 communication protocol.

48. The packet-based switch of claim 47 wherein the switch comprises plural ports.

49. The packet-based switch of claim 47 wherein the switch comprises at least 4 ports.

50. The packet-based switch of claim 47 wherein the switch comprises at least 8 ports.

51. The packet-based switch of claim 45 wherein the number of memory accesses required per Ethernet frame is one of:

a. one cycle per frame for address resolution;
b. one cycle per frame for address learning;
c. one cycle per frame for transmission read;
d. one cycle per frame for transmission write;
e. one cycle per eight bytes for a frame data read; and
f. one cycle per eight bytes for a frame data write.

52. A packet-based switch comprising an Address Resolution Table having a one-way associative memory structure and a Packet Data Buffer Table sharing a memory block with the Address Resolution Table.

53. The packet-based switch of claim 52 wherein the switch comprises plural ports.

54. The packet-based switch of claim 52 wherein the switch comprises at least 4 ports.

55. The packet-based switch of claim 52 wherein the switch comprises at least 8 ports.

56. The packet-based switch of claim 52 wherein the number of memory accesses required per Ethernet frame is one of:

a. one cycle per frame for address resolution;

b. one cycle per frame for address learning;

c. one cycle per frame for transmission read;

d. one cycle per frame for transmission write;

e. one cycle per eight bytes for a frame data read; and

f. one cycle per eight bytes for a frame data write.

57. A packet-based switch, comprising an Address Resolution Table having a direct-mapped/one-way associative memory structure, the Address Resolution Table for resolving addresses in a packet-based network switch.

58. The packet-based switch of claim 58 wherein the direct-mapped/one-way associative memory is searched using a destination address key direct-mapped address search.

59. The packet-based switch of claim 58 wherein the switch implements an IEEE Standard 802.3 communication protocol.

60. The packet-based switch of claim 59, wherein the switch comprises plural ports.

34556/JFO/B600

MEMORY STRUCTURE

ABSTRACT OF THE DISCLOSURE

Memory structure, and packet-based switch including the memory structure, having Address Resolution Table and Packet Data Buffer table employing a shared memory. Transmit Descriptor Table also may share memory. Address Resolution Table can be implemented with direct mapping, for which destination address key direct-mapped address search may be used. The memory structure and switch implement an IEEE Std. 802.3 communication protocol via multiple ports.

JFO/llb

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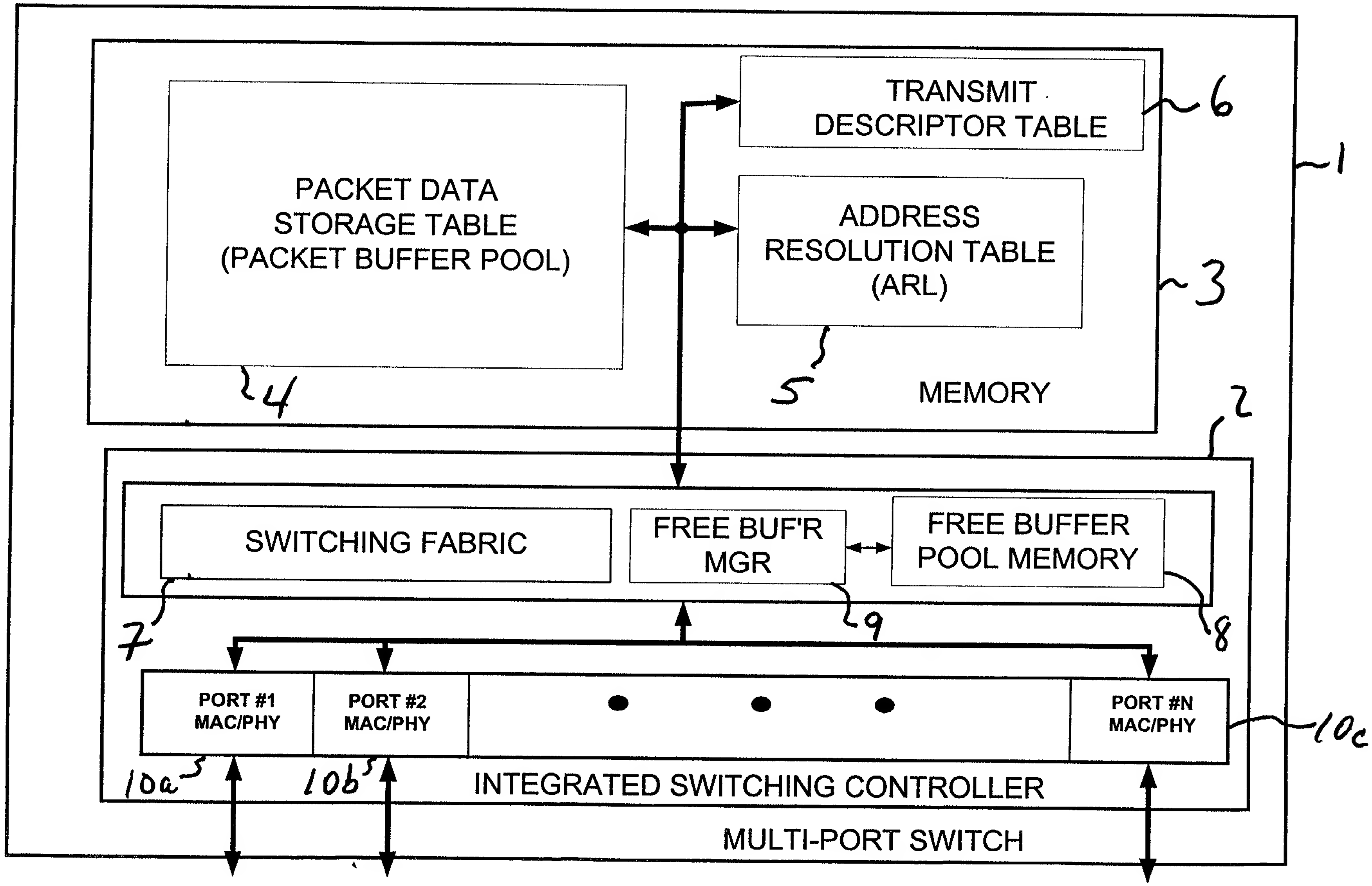


FIGURE 1

100

	Address[7:0]	Data[63:0]	
11	00-CF	Packet Data	12
13	D0	Port 0 Transmit Descriptor	14
	D1	Port 1 Transmit Descriptor	
	D2	Port 2 Transmit Descriptor	
	D3	Port 3 Transmit Descriptor	
	D4	Port 4 Transmit Descriptor	
	D5	Port 5 Transmit Descriptor	
	D6	Port 6 Transmit Descriptor	
	D7	Port 7 Transmit Descriptor	
15	D8	Port 8 Transmit Descriptor	16
	D9-DF	Unused	
17	E0-FF	32 ARL Table Entries	18

FIGURE 2

	Address[16:0]	Data[63:0]	
19	0000-00FF	Memory Block 0	20
	0100-01FF	Memory Block 1	
	0200-02FF	Memory Block 2	
	0300-FEFF	Memory Block 3 to 2046	
	FF00-FFFF	Memory Block 2047	
	10000-1FFFF	Optional Memory Block 2048-4095	

FIGURE 3

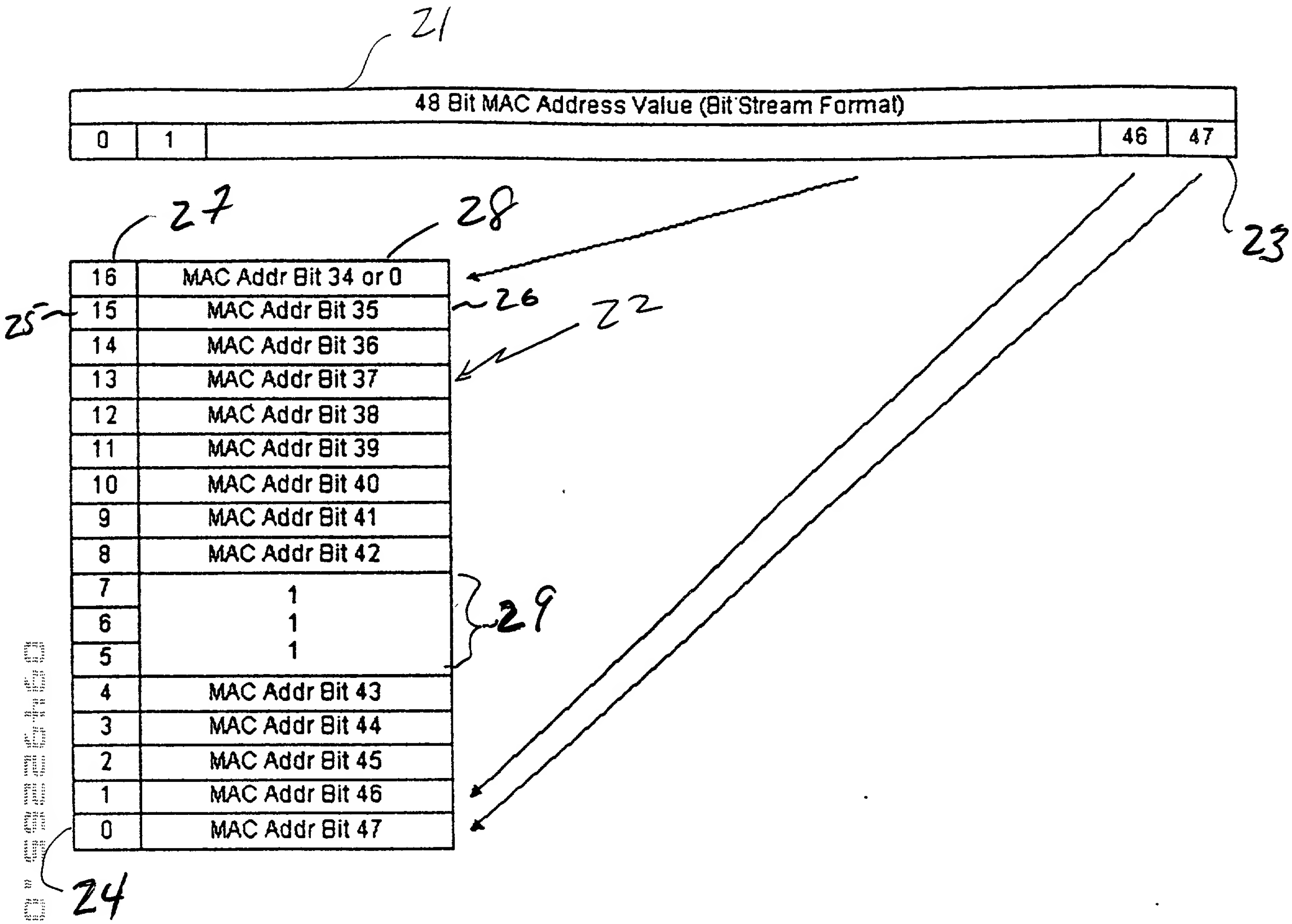


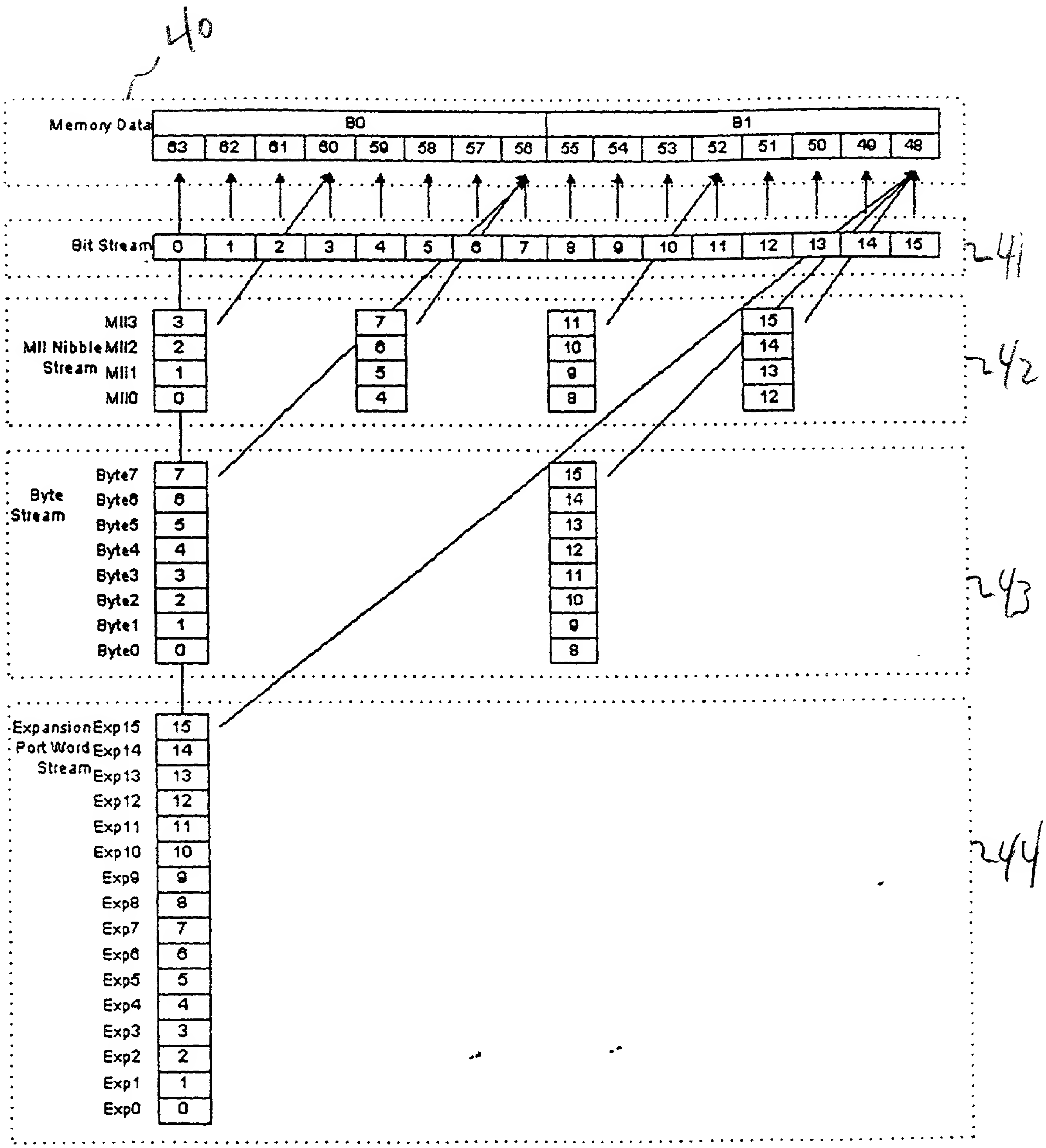
FIGURE 4

31 30 32

Address[7:0]	Data[63:0]							
	[63:56]	[55:48]	[47:40]	[39:32]	[31:24]	[23:16]	[15:8]	[7:0]
00	B0	B1	B2	B3	B4	B5	B6	B7
01	B8	B9	B10	B11	B12	B13	B14	B15
..	-	-	-	-	-	-	-	-
07	B56	B57	B58	B59	B60	B61	B62	B63
08	B64	B65	Unused					
08-CF	Unused							

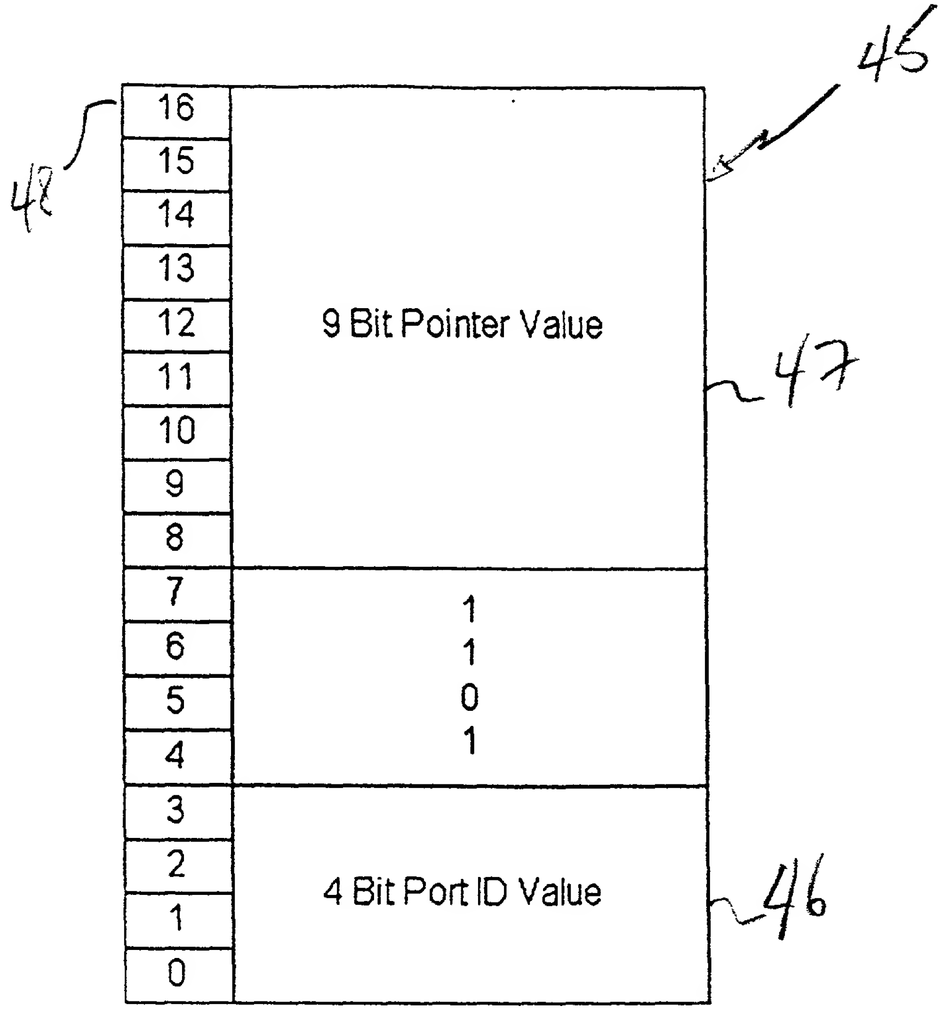
33 34 36 35

FIGURE 5



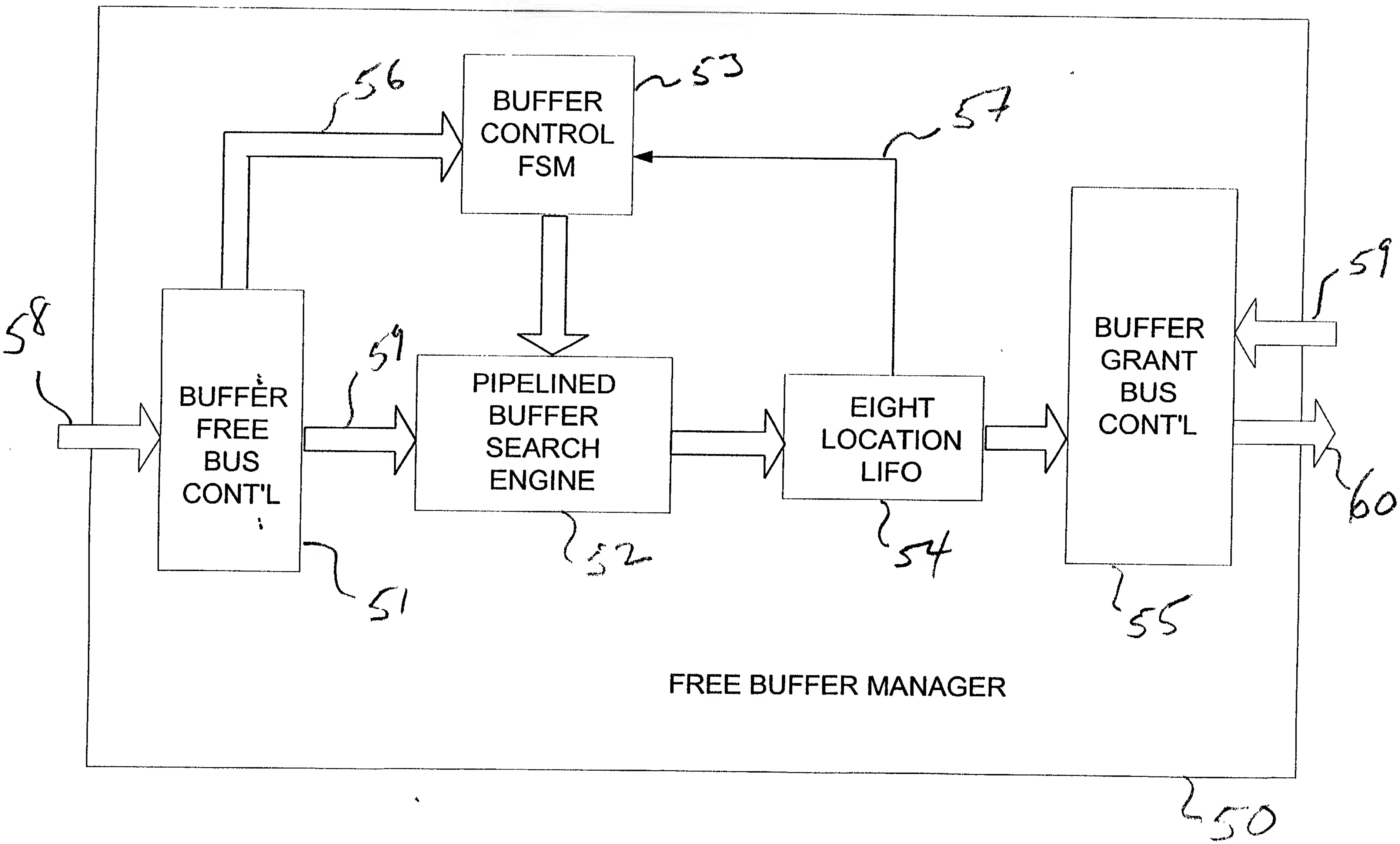
40
Memory Data
B0
B1
63
62
61
60
59
58
57
56
55
54
53
52
51
50
49
48
Bit Stream
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
41
MII Nibble Stream
MII3
MII2
MII1
MII0
42
Byte Stream
Byte7
Byte6
Byte5
Byte4
Byte3
Byte2
Byte1
Byte0
43
Expansion Port Word Stream
Exp15
Exp14
Exp13
Exp12
Exp11
Exp10
Exp9
Exp8
Exp7
Exp6
Exp5
Exp4
Exp3
Exp2
Exp1
Exp0
44

FIGURE 6



Transmit Descriptor Pointer Address

FIGURE 7



58
BUFFER FREE BUS CONT'L
51
59
56
BUFFER CONTROL FSM
53
PIPELINED BUFFER SEARCH ENGINE
52
57
EIGHT LOCATION LIFO
54
BUFFER GRANT BUS CONT'L
55
59
60
FREE BUFFER MANAGER
50

FIGURE 8

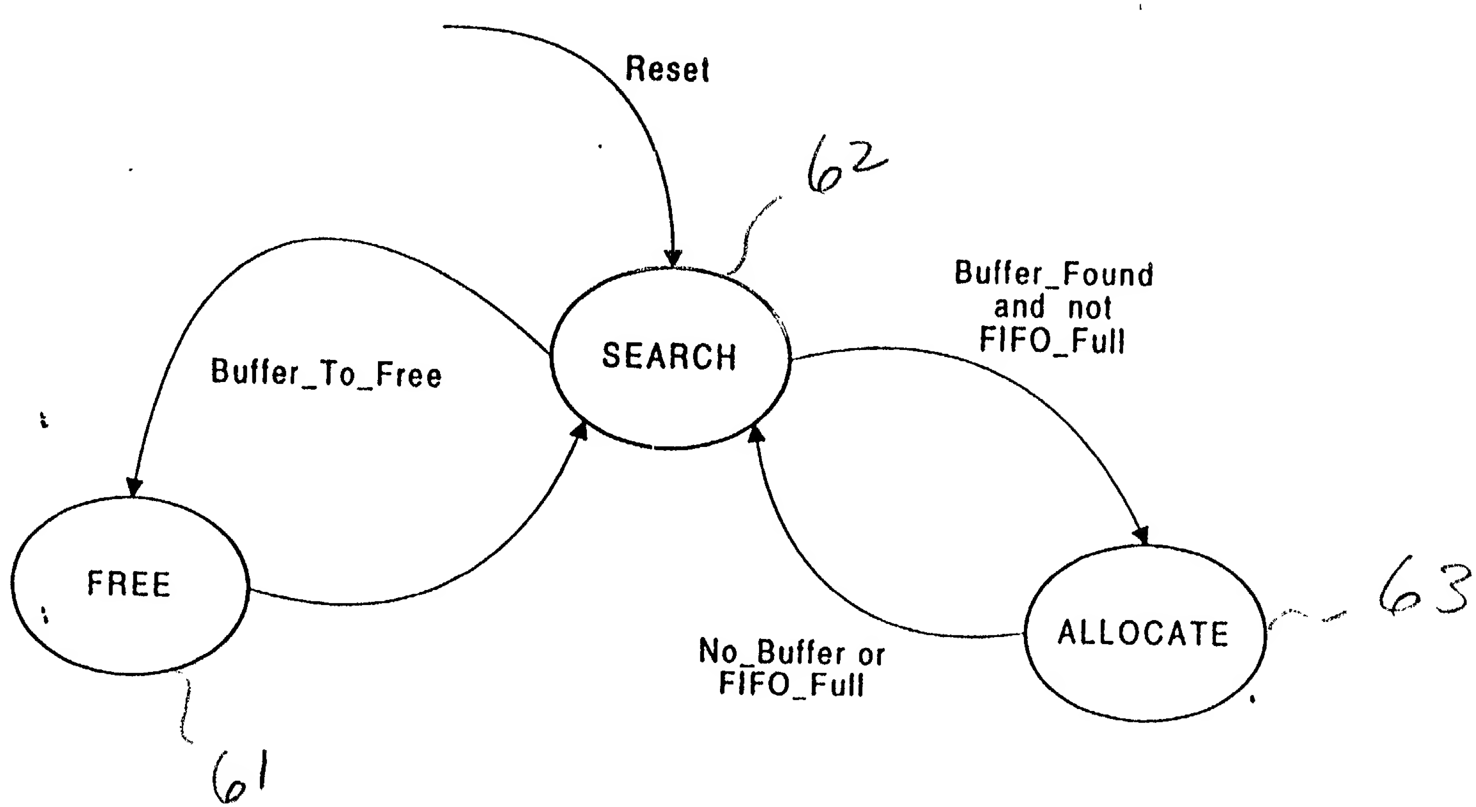

Reset
SEARCH
62
Buffer_To_Free
Buffer_Found
and not
FIFO_Full
FREE
ALLOCATE
63
No_Buffer or
FIFO_Full
61

FIGURE 9

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATIONS

PATENT

Docket No. : 34556/JFO/B600

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **MEMORY STRUCTURE**, the specification of which is attached hereto unless the following is checked:

__ was filed on ________________________ as United States Application Number ____________________ or PCT International Application Number __ and was amended on __ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of the foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Application Number	Country	Filing Date (day/month/year)	Priority Claimed

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

Application Number	Filing Date
60/117,481	**January 27, 1999**
60/127,147	**March 31, 1999**

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

Application Number	Filing Date	Patented/Pending/Abandoned

POWER OF ATTORNEY: I hereby appoint the following attorneys and agents of the law firm CHRISTIE, PARKER & HALE, LLP to prosecute this application and any international application under the Patent Cooperation Treaty based on it and to transact all business in the U.S. Patent and Trademark Office connected with either of them in accordance with instructions from the assignee of the entire interest in this application;

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATIONS

Docket No. 34556/JFO/B600

or from the first or sole inventor named below in the event the application is not assigned; or from __ in the event the power granted herein is for an application filed on behalf of a foreign attorney or agent.

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I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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FOR PATENT APPLICATIONS

Docket No. 34556/JFO/B600

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